

## WHAT IS CLAIMED IS:

- 1 1. A computer system having a common display memory and main memory,  
2 comprising:  
3 a display means;  
4 a first plurality of internal and external memory subsystems;  
5 a second plurality of memory channels;  
6 a memory channel data switch and controller unit for allocating the memory  
7 channels among a plurality of subsystems;  
8 a central processing unit (CPU) subsystem controller unit producing output  
9 signals to be applied to the memory channel data switch and controller unit;  
10 a graphics/drawing and display subsystem producing output signals to be applied  
11 to the memory channel data switch and controller unit;  
12 an arbitration and control unit producing output signals to be applied to the CPU  
13 subsystem controller unit and to the graphics/drawing and display subsystem;  
14 a peripheral bus control unit producing output signals to be applied to the memory  
15 channel data switch and controller unit and to the arbitration and control unit; and  
16 a direct input/output (I/O) control unit producing output signals to be applied to  
17 the memory channel data switch and controller unit and to the arbitration and control unit.
- 1 2. The computer system of claim 1 further comprising multiplexer means for  
2 multiplexing said external memory subsystems into at least one memory channel.

1 3. The computer system of claim 1 wherein one of said memory subsystems is a  
2 display memory which can also function as a main system memory.

1 4. The computer system of claim 1 wherein at least one of said memory subsystems  
2 includes a data manipulator containing a plurality of storage elements.

1 5. The computer system of claim 1 wherein said graphics/drawing subsystem can  
2 draw directly into any area of said main memory.

1 6. The computer system of claim 1 wherein said peripheral bus can transfer data into  
2 said main memory, and said graphics/drawing and display subsystem can utilize display  
3 refresh data without storing a copy of the display refresh data and without using a CPU.

1 7. The computer system of claim 1 further comprising a partial drawing buffer where  
2 a graphics engine can write a portion of the display output data and transfer the portion of  
3 the display output data to a common memory subsystem for use during subsequent  
4 display updates after a display frame has been processed.

1 8. The computer system of claim 1 further comprising a complete drawing buffer  
2 where a graphics engine can store the complete display output data and transfer the  
3 display output data for subsequent display updates.

1 9. The computer system of claim 1 further comprising:  
2 a graphics controller for performing 3-D graphics functions; and  
3 a texture cache from which the graphics controller can fetch data.

1 10. The computer system of claim 1 further comprising:  
2 separate controllers for each memory subsystem;  
3 an arbiter that takes requests from multiple subsystems; and  
4 a memory data path through which a memory subsystem can provide memory  
5 data to a subsystem without preventing other subsystems from accessing other memory  
6 subsystems.

1 11. The computer system of claim 1 further comprising:  
2 at least one graphics engine; and

3 at least one partial drawing buffer into which said at least one graphics engine can  
4 write a portion of display output data and transfer the portion of display output data for  
5 subsequent display updates.

1 12. The computer system of claim 1 further comprising:  
2 a graphics controller for performing 3-D graphics functions; and  
3 an order buffer from which said graphics controller can fetch data.

1 13. A computer system having a common display memory and main memory,  
2 comprising:  
3 a display means;  
4 a first plurality of internal and external memory subsystems;  
5 a second plurality of memory channels;  
6 a memory channel data switch and controller unit for allocating the memory  
7 channels among a plurality of subsystems;  
8 a central processing unit (CPU) subsystem controller unit producing output  
9 signals to be applied to the memory channel data switch and controller unit;

10 a graphics/drawing and display subsystem producing output signals to be applied  
11 to the memory channel data switch and controller unit;  
12 an arbitration and control unit producing output signals to be applied to the CPU  
13 subsystem controller unit and to the graphics/drawing and display subsystem; and  
14 a peripheral bus control unit producing output signals to be applied to the memory  
15 channel data switch and controller unit and to the arbitration and control unit.

1 14. The computer system of claim 13 further comprising multiplexer means for  
2 multiplexing said external memory subsystems into at least one memory channel.

1 15. The computer system of claim 13 wherein one of said memory subsystems is a  
2 display memory which can also function as a main system memory.

1 16. The computer system of claim 13 wherein at least one of said memory subsystems  
2 includes a data manipulator containing a plurality of storage elements.

1 17. The computer system of claim 13 further comprising a complete drawing buffer  
2 where a graphics engine can store the complete display output data and transfer the  
3 display output data for subsequent display updates.

1 18. The computer system of claim 13 further comprising:  
2 a graphics controller for performing 3-D graphics functions; and  
3 a texture cache from which the graphics controller can fetch data.

1 19. The computer system of claim 13 further comprising:  
2 separate controllers for each memory subsystem;  
3 an arbiter that takes requests from multiple subsystems; and  
4 a memory data path through which a memory subsystem can provide memory  
5 data to a subsystem without preventing other subsystems from accessing other memory  
6 subsystems.

1 20. The computer system of claim 13 further comprising:  
2 a graphics controller for performing 3-D graphics functions; and  
3 an order buffer from which said graphics controller can fetch data.

1 21. The computer system of claim 13 further comprising:  
2 separate controls for each memory subsystem;  
3 an arbiter that takes requests from multiple processor or peripheral subsystems;  
4 and  
5 a memory data path wherein memory data can be provided by a memory  
6 subsystem to a processor or peripheral subsystem without preventing additional processor  
7 or peripheral subsystems from accessing other memory subsystems.

1 22. The computer system of claim 13 further comprising:

2 an integrated processor that receives input data from the memory channel data  
3 switch and controller unit and that provides output data to an input of the arbitration and  
4 control unit.

1 23. A computer system having a common display memory and main memory,  
2 comprising:  
3 a display means;  
4 a plurality of internal and external memory subsystems, each having its own  
5 memory channel;  
6 a memory channel data switch and controller unit wherein the memory channels  
7 can be allocated to a plurality of processor or peripheral subsystems;  
8 a CPU subsystem controller unit producing output signals received proportionally  
9 by the memory channel data switch and controller unit; and  
10 an arbitration and control unit producing output signals received proportionally by  
11 the CPU subsystem controller unit.

1 24. An computer system having a plurality of internal and external memory  
2 subsystems comprising:  
3 multiple concurrent memory channels;  
4 a memory channel data switch and controller unit wherein the memory channels  
5 can be allocated to a plurality of processor or peripheral subsystems;

a means for a plurality of processors and peripheral subsystems to access the common memory regions; and

at least one of the internal memory subsystems is DRAM memory.

25. The computer system of claim 24 further comprising:

a multi-bank internal DRAM memory;

a means for multiple processor or peripheral subsystems to access a plurality of the banks; and

a means for an arbiter to allow multiple processor or peripheral subsystems to serially access a given bank of memory.

26. The computer system of claim 24 further comprising:

- a bank of internal DRAM memory with multiple row buffers;

a means for multiple processor or peripheral subsystems to access a plurality of the row buffers; and

a means for an arbiter to allow multiple processor or peripheral subsystems to serially access a given row buffer.

27. A monolithic integrated circuit comprising:

at least one internal memory subsystem of DRAM memory;

at least one external memory control for DRAM memory;



4 a plurality of concurrent memory channels; and  
5 a means for multiple compute engines, multiple processors or peripheral  
6 subsystems to access the memory channels;

1 28. The monolithic integrated circuit of claim 27 where multiple compute engines  
2 concurrently access said internal memory subsystem of DRAM memory through a data  
3 switch to a plurality of banks of memory.

1 29. The monolithic integrated circuit of claim 27 where a plurality of compute  
2 engines concurrently access said internal memory subsystem of DRAM memory through  
3 a data switch to a plurality of row buffers.

1 30. The monolithic integrated circuit of claim 27 where at least one of the said  
2 internal memory subsystems of DRAM memory includes a data manipulator containing a  
3 plurality of storage elements as well as a simple Arithmetic Logic Unit (ALU).

1 31. A computer system having a common display memory and main memory,  
2 comprising:  
3 a display means;  
4 a plurality of internal and external memory subsystems;  
5 a central processing unit (CPU) subsystem controller unit producing output  
6 signals;  
7 a graphics/drawing and display subsystem producing output signals;

8           an arbitration and control unit producing output signals to be applied to the CPU  
9           subsystem controller unit and to the graphics/drawing and display subsystem; and  
10           a peripheral bus control unit producing output signals to be applied to the CPU  
11           controller unit and to the arbitration and control unit.

1   32.    The computer system of claim 31 further comprising:

2           a graphics controller for performing 3-D graphics functions; and  
3           a texture cache from which the graphics controller can fetch data.

1   33.    The computer system of claim 31 further comprising:

2           a graphics controller for performing 3-D graphics functions; and  
3           an order buffer from which said graphics controller can fetch data.